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UNITED STATES PATENT APPLICATION
FOR

STRESS-TEST INFORMATION DATABASE STRUCTURE
AND METHOD OF USE

BY

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Certification Under 37 C.F.R. Section 1.10

I hereby certify that this New Application Transmittal Letter and the documents referred to as being enclosed therein are being deposited with the United States Postal Service on this 11th day of October, 2001 in an envelope marked as "Express Mail Post Office to Addressee" Mail Label Number EL869632542US addressed to Box Patent Application, Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Carol S. Parker-Hines

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STRESS-TEST INFORMATION DATABASE STRUCTURE AND METHOD OF USE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of priority under 35 U.S.C. § 119(e) to U.S. Provisional Application Serial No. 60/240,596 filed on October 13, 2000 the entirety of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of Invention

The invention relates to methods and systems for performing stress testing of equipment. The invention also relates to active and passive stress testing using modular design and robust data collection that is adaptable to a variety of equipment.

Description of Related Art

It is common to subject integrated circuits (IC) to various stresses to ensure reliability. Specifically, an IC is typically subjected to high temperatures for an extended period of time. This process is called "burn-in" testing in the art and identifies marginal devices likely to succumb to such stresses in the field.

Various systems and methods have been designed to perform burn-in testing of integrated circuits and computer components. Many of these conventional solutions focus on specific adapters and hardware that permit high-volume burn-in testing of specific equipment.

For example, Slocum (USP 6,097,201) discloses a system of stackable test boards in which a large number of integrated circuit boards may be mounted. Each of Slocum's test boards includes a contactor region that permits test signals to be routed to the individual integrated circuit boards. As such, Slocum's system is specifically designed to perform high-volume burn-in testing of specific components (integrated circuit boards).

Leung (USP 5,798,653) utilizes a special-purpose burn-in controller located within the burn-in oven to "exercise" an integrated circuit (IC) by toggling a high percentage of the switches within the IC.

Leung also illustrates the conventional thinking of burn-in testing which is to select a statistically significant sample of the product (IC's in this case) which are then subjected to burn-in testing. Like Slocum, Leung's system performs a dynamic test in which input stimuli are applied to the ICs to exercise or toggle the electrical circuit nodes of the IC.

Leung performs two types of dynamic burn-in testing on these sample IC's including an infant mortality burn-in and a longevity qualifying burn-in which mainly differ in the amount of time in which the IC's are subjected to the age-accelerating burn-in test. A simple data set is collected from these tests, which includes how many ICs succumb to infant mortality.

The flexibility of conventional stress testing systems is quite limited. Moreover, the number testing circuits matches the number of IC boards being tested thus requiring duplicative testing hardware. Moreover, the data collected by conventional system is quite rudimentary. Thus, there is a need in the art that solves these and other deficiencies in conventional stress-testing systems.